WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory cells arranged in rows and columns;

a plurality of sub word lines, provided corresponding to the respective memory cell rows, each having memory cells on a corresponding row connected thereto;

a plurality of main word lines, each provided corresponding to a prescribed number of sub word lines in said plurality of sub word lines and disposed in a first conductive layer, for transmitting a row select signal;

a plurality of shunting interconnection lines, provided corresponding to the respective sub word lines in a second conductive layer formed under said first conductive layer, each for electrically connecting to a corresponding sub word line at a prescribed interval; and

a plurality of sub word drivers, provided corresponding to the sub word lines, each for driving a corresponding sub word line and a corresponding shunting interconnection line into a selected state according to at least a row select signal on a corresponding main word line.

2. The semiconductor memory device according to claim 1, wherein said first conductive layer is a third level metal interconnection layer and said second conductive layer is a first level metal interconnection layer.

3. The semiconductor memory device according to claim 1, wherein each of said plurality of sub word lines is electrically connected to a corresponding shunting interconnection line at both opposed ends thereof.

4. The semiconductor memory device according to claim 1, further comprising an intermediate voltage transmission line, formed in a third conductive layer different from the first and second conductive layers, for transmitting an intermediate voltage at a prescribed voltage level.

5. The semiconductor memory device according to claim 4, wherein

said third conductive layer is a second level metal interconnection line formed in an interconnection layer between the first and second conductive layers.

6. The semiconductor memory device according to claim 4, wherein each memory cell has a capacitance for storing information and said intermediate voltage is applied to a reference power supply node of said capacitance.

7. The semiconductor memory device according to claim 6, wherein said reference power supply node is formed under said second conductive layer, said third conductive layer is electrically connected to said reference power supply node through a metal interconnection line formed in said second conductive layer.

8. The semiconductor memory device according to claim 1, wherein said plurality of sub word lines are grouped into a plurality of groups along a row direction and

said plurality of sub word drivers performs a select operation in units of the groups.

9. The semiconductor memory device according to claim 1, further comprising a power supply line, disposed in an interconnection layer different from said first conductive layer over a memory cell array in which said plurality of memory cells are arranged, for transmitting a power supply voltage.

10. The semiconductor memory device according to claim 1, wherein said semiconductor memory device is an embedded memory integrated with a logic circuit on a common semiconductor substrate.

11. The semiconductor memory device according to claim 1, wherein the metal interconnection line is a copper interconnection line.